Metal oxide Semiconductor Field Effect Transistor (MOSFET)

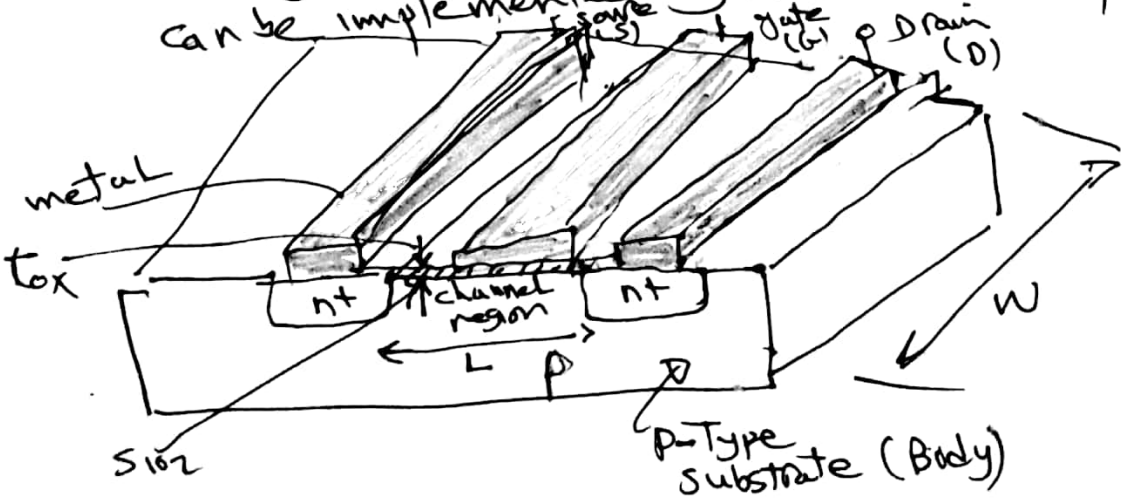
- Diode is Two Terminal device
- Three Terminal device such as BJT MOSFET are more useful Than Two terminal device
- Three Terminal devices are used in multitude of applications ranging from Signal amplification To digital logic and memory.
- idea is use voltage between 2 Terminal To control current in Third Terminal, so it can be as Controlled Source

application of MOSFET + its properties over BJT

- Design of I'Cs, so entire circuits y single chip
- occupies small volume, size (> $4*10^{12}$ TRx/chip)
- Their operation require little power

idea ⇒ start by Julius E. liliemfeld in 1925
⇒ appear by William Shockely in 1952
⇒ Bell lab produce 1st TRANSISTOR at 1960

- very large scale integrated (VLSI) digital Circuit such as microprocessor, memory are use MOSFET
- analog circuit such as amplifiers + filter can be implemented by MOS Technology



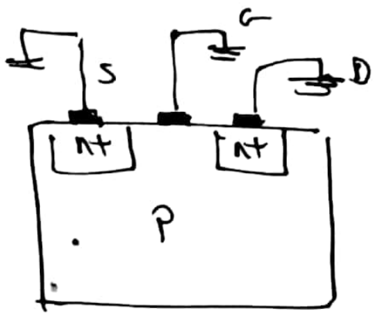
Terminals are gate (G)
Drain (D)
Source (S)

Typicall values
- L channel length [0.03 μm → 1 μm]
- W ~ width [0.05 μm → 100 μm]
- t_{ox} SiO_2 Thickness [1nm → 10 nm]

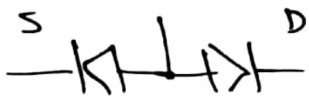
MOSFET is called also insulated-gate FET (IGFET)
where $I_G \simeq 10^{-15}$ A which is very small.

عن طريق جهد الـ gate يتم التحكم في التيار المار بين S ، D

(a) when $V_{GS} = 0$



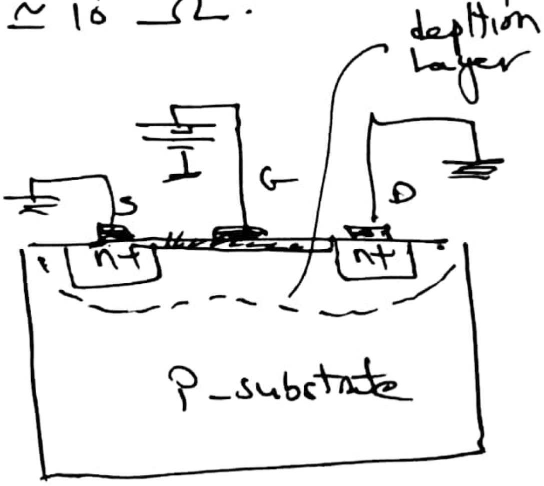
like



So No Current flow from drain To source.

when V_{DS} ↑ , There is very high resistance between drain & Source $R_{DS} \simeq 10^{12}\,\Omega$.

(b) when $V_{GS} = +ve$



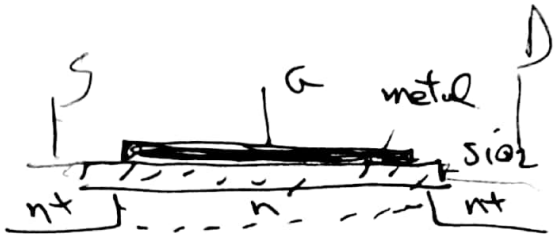
as V_G is +ve
(1) hole under SiO_2 layer will repel To down so channel is free from holes so called (depltion Layer)

ويصبح منطقة depltion region غنية بـ bound -ve charge وهذه الشحنات لا تتأثر
وذلك لإزالة الـ holes إلى أسفل في الـ p-substrate

(2) +ve on gate attracte n^+ from D, S

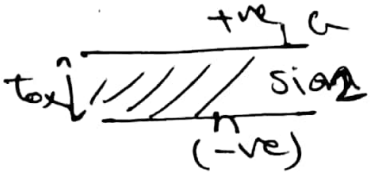
عند الـ V_{GS} اللي عنده تتكون channel يسمى Threshold voltage
V_{Th} [0.1 → 0.3 V] for NMOS.

If an voltage applied between D,S, so current will flow



In Fact

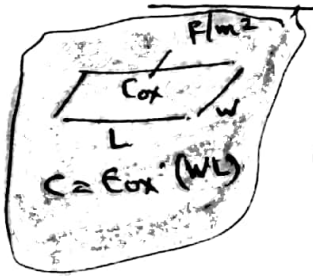
gate metal + n-channel + SiO2 Construct Capacitor or parallel plate capacitor.



Field Effect Transistor (FET)

V_{GS} must be $> V_t$ To construct channel so any voltage of V_{GS} above V_t called overdrive voltage $V_{OV} = V_{GS} - V_t$

Electron charge in channel



$$|Q| = C_{ox}(WL)V_{OV}$$

where $\because Q = CV$

C_{ox} ⇒ oxide capacitance / unit area (F/m^2)

W ⇒ channel width

L ⇒ channel length

since $C = \frac{\epsilon A}{d}$ $\therefore C_{ox} = \frac{C}{A} = \frac{\epsilon_{ox}}{t_{ox}}$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

ϵ_{ox} ⇒ silicon dielectric constant $\simeq 3.9\,\epsilon_0$

$= 3.45 * 10^{-11}$ F/m

t_{ox} ⇒ SiO_2 (silicon oxide thickness)

when $t_{ox} = 4nm$ $\therefore C_{ox} = \frac{3.45*10^{-11}}{4*10^{-9}} = 8.6*10^{-3}$ F/m

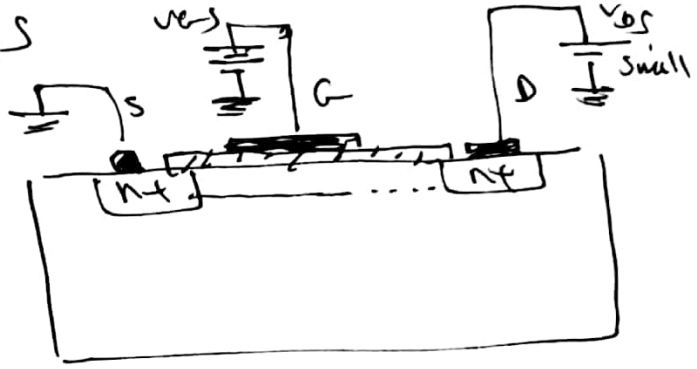
3/10

$\frac{W}{L}$ ⇒ aspect ratio

when $L = 0.18\ \mu m$
$W = 0.72\ \mu m$

$$C = C_{ox} WL = 8.6*10^{-3} * 0.72*10^{-6} * 0.18*10^{-6}$$
$$= 1.1*10^{-15}\ F = 1.1\ fF$$

(c) applying a small V_{DS}



as V_{DS} is +ve & small
V_{DS} cause electron to move through channel for source to drain so current from Drain To Source appear (I_{DS})

voltage between gate & different points on channel is equal To V_{ov}

$$\therefore \frac{\text{charge}}{\text{unit channel length}} = \frac{|Q|}{L} = \frac{C_{ox} WL V_{ov}}{L}$$
$$= C_{ox} W V_{ov}$$

In fact V_{DS} cause an electric field across the channel $|E| = \frac{V_{DS}}{L}$

This field (E) cause electron in channel moves with drift velocity V_d

Electron drift velocity $V_d = \mu_n |E|$
$= \mu_n \frac{V_{DS}}{L}$

μ_n ⇒ electron mobility at channel surfaces

4/10
L252

$$i_D = \frac{\text{charge}}{\text{unit length}} * v_d \qquad \left(\frac{C}{m} \cdot \frac{m}{s} = \frac{C}{s} \equiv A\right)$$

$$= \frac{C_{ox} W L\ V_{ov}}{L} * \mu_n \frac{V_{DS}}{L}$$

$$= \left[\mu_n C_{ox} \left(\frac{W}{L}\right) V_{ov}\right] V_{DS} = \left[\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)\right] V_{DS}$$

Trans conductance between Drain & source

$$g_{DS} = \frac{\partial i_D}{\partial V_{DS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)$$
$$= \mu_n C_{ox} \frac{W}{L} V_{ov}$$

conductance g_{DS} α
1. $\mu_n C_{ox}$
2. $\frac{W}{L}$
3. $(V_{GS} - V_T)$

[1] $\mu_n C_{ox}$ ⟹ determined by process (Technology of fabrication)

$$K_n' = \mu_n C_{ox} \qquad \left[\frac{m^2}{V \cdot S} \cdot \frac{F}{m^2} = \frac{F}{V \cdot S} = \frac{C/V}{V \cdot S} = \frac{A}{V^2}\right]$$

$$\therefore i_D = K_n' \left(\frac{W}{L}\right) (V_{GS} - V_T) V_{DS}$$
$$= K_n (V_{GS} - V_T) V_{DS}$$

[2] $\frac{W}{L}$ ⟹ aspect ratio [can be design by designer based on required

$\frac{W}{L}$ Linked to < Transconductance / current capability Together with multiplicity (m)

as $\frac{W}{L}$ ↑ as current gain ↑ for given V_g

example ① for op-amp need higher gain in input stage so $\frac{W}{L}$ high is useful

② in current mirror higher L is useful for matching of mirror current

In fact larger Transistor (due To increase of L) ensure better matching due To minimization of edge effect

minimum $\frac{W}{L}$ is 2.5 for NMOS & > 2.5 for PMOS

في الواقع التكنولوجيا تم تحديدها بناء على اقل length كانت تصنيعه هو اقل Lmin) [تصنيعه min length

1996 – 1998	⟹	Lmin = 250 nm	T_{ox} ↓
2000 – 2002	⟹	Lmin 130 nm	
2003 – 2005	⟹	Lmin = 90 nm	
2014	⟶	Lmin 32 nm	T_{ox} = 2.2 nm
2016	⟶	Lmin 6.5 nm	
2019	⟶	Lmin = 5 nm	by Samsung electronic

as L ↓ as # of chips per wafer ↑ [# of Transistor per chip double every 2–3 year

في الواقع كلما صغرت L كلما تحتاج إلى V_T أقل وتظهر مشاكل تخص gate oxide leakage reverse-bias injection

ط/5
L252

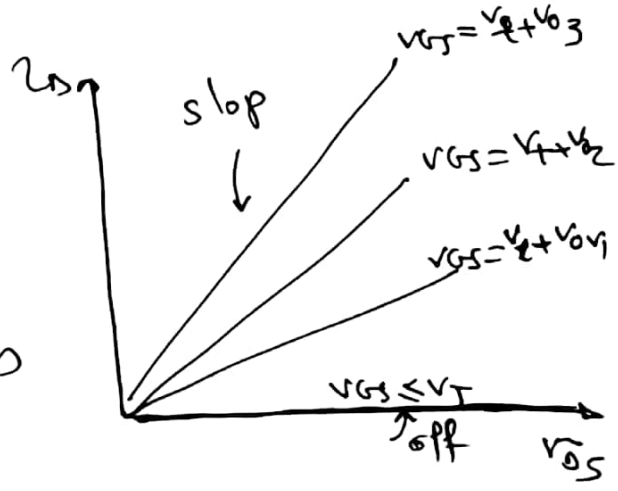
$$K_n = \mu_n C_{ox} \frac{W}{L} = \acute{K}_n \frac{W}{L} \quad \left(\frac{A}{V^2}\right)$$

Factor-3 ③ $(V_{GS} - V_T)$ or V_{ov}

V_{ov} is very important parameter and used in design of what need?

$$r_{DS} = \frac{1}{g_{ds}} = \frac{1}{\mu_n C_{ox} \frac{W}{L} V_{ov}} = \frac{1}{\acute{K}_n \frac{W}{L} V_{ov}}$$

$$r_{ds} = \frac{1}{K_n V_{ov}} = \frac{1}{K_n (V_{GS} - V_T)}$$



$$\text{slop} \simeq \frac{1}{r_{ds}}$$

or $\text{slop} \equiv g_{ds} = K_n V_{ov}$

as $V_{ov} \downarrow$ as slop $\downarrow$ as $g_{ds} \downarrow$ as $r_{ds} \uparrow$

In This case $v_{D_{sam}} = v_{S_{source}}$ where $v_G = 0$

(EX) For 0.18 μm Fabrication Technology, $t_{ox} = 4.1$ nm

$\mu_n = 450 \frac{cm^2}{V^2}$, $V_t = 0.5$ V

(a) Find $\acute{K}_n$ (b) when use L_{min}, find W To have $r_{ds} = 1$ kΩ at $V_{GS} = 1$ V

Given $\varepsilon_{ox} = 3.9 \varepsilon_0$

(a) $\acute{K}_n = \mu_n C_{ox} = \mu_n \frac{\varepsilon_{ox}}{t_{ox}} = 450 \frac{cm^2}{V^2} * \frac{3.9 * 8.85 * 10^{-12} \frac{F}{m}}{4 * 10^{-9} m}$

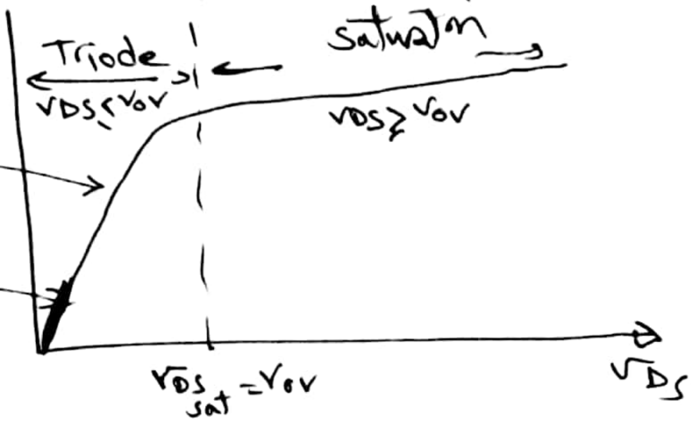
$= 450 * 10^{-4} \frac{m^2}{V^2} * \frac{3.9 * 8.85 * 10^{-12} \frac{F}{m}}{4 * 10^{-9} m}$

$= 388.47 \ \mu A/V^2$

$\because r_{ds} = \frac{1}{\acute{K}_n \frac{W}{L} (V_{GS} - V_T)}$

$\therefore \frac{W}{L} = \frac{1}{\acute{K}_n r_{ds} (V_{GS} - V_T)}$

MOSFET Region



channel بسبب انحناء المنحنى هو انه مقاومة
تزيد مع زيادة VDS

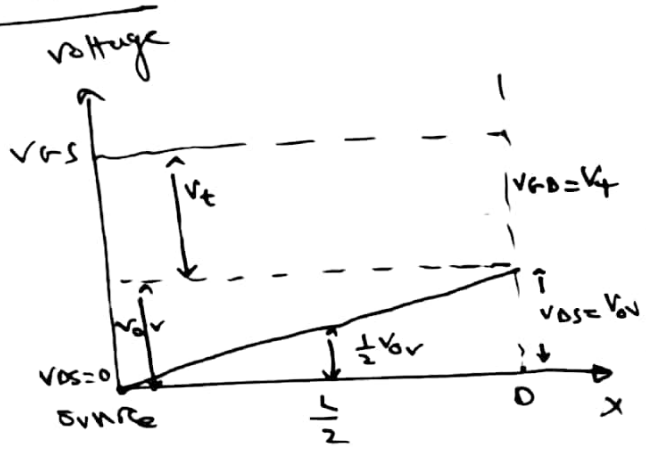
عندما يكون VDS صغيراً جداً بيكون خط
مستقيم لانه المقاومة ثابتة لان الجهد في كل نقاط
الـ channel ثابت

$$\therefore i_D = k_n' \frac{W}{L}\left(V_{ov} V_{DS} - \frac{V_{DS}^2}{2}\right)$$

$$i_D = k_n' \frac{W}{L}\left[(V_{GS}-V_t) V_{DS} - \frac{V_{DS}^2}{2}\right]$$

معادلة تيار Triode region

operation for $V_{DS} \geq V_{ov}$ (saturation)



channel area $\propto \frac{V_{ov} + 0}{2}$

$\propto \frac{V_{ov}}{2}$

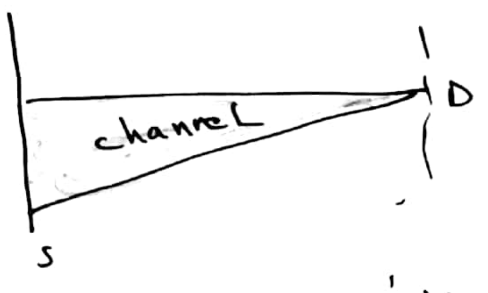
$\therefore i_D \propto k_n' \frac{W}{L} V_{DS} * \frac{V_{ov}}{2}$

since at Drain $V_{DS} = V_{ov}$

$$i_D = k_n' \frac{W}{L} \frac{V_{ov}^2}{2}$$

$$= \frac{1}{2} k_n' \frac{W}{L} V_{ov}^2$$

$$i_{D\,sat} = \frac{1}{2} k_n' \frac{W}{L} (V_{GS}-V_t)^2$$ معادلة



الخلاصة

Triode	Sat
$V_{DS} < V_{GS}-V_T$	$V_{DS} \geq V_{GS}-V_T$
$i_D = k_n' \frac{W}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$	$i_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS}-V_t)^2$
$= k_n' \frac{W}{L}\left[V_{ov}V_{DS} - \frac{V_{DS}^2}{2}\right]$	$= \frac{1}{2} k_n' \frac{W}{L} V_{ov}^2$

8/10
L2S2

(Ex) Consider a process Technolog for $L_{min} = 0.4\mu m$
$t_{ox} = 8.nm$
$\mu_n = 450 cm^2/V.s$
$V_t = 0.7V$

(a) find C_{ox}, K_n'

(b) For $\frac{W}{L} = \frac{8\mu m}{0.8\mu m}$, Calculate V_{ov}, V_{GS}, $V_{DS\,min}$ need to operate in sat region, $I_D = 100\mu A$

(c) Find V_{ov}, V_{GS} require to Cause $r_{DS} = 1000\Omega$ when V_{DS} is small

(a)

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\varepsilon_0}{t_{ox}} = \frac{3.9 * 8.854 * 10^{-12}\ F/m}{8 * 10^{-9}} = 4.32 * 10^{-3}\ F/m^2$$

$$K_n' = \mu_n C_{ox} = 450\frac{cm^2}{V.s} * 4.32 * 10^{-3}\frac{F}{m^2}$$

$$\left[\frac{F}{V.s} = \frac{C/V}{V.s} = \frac{A}{V^2}\right]$$

$$= 450 * 10^{-4}\frac{m^2}{V.s} * 4.32 * 10^{-3}\frac{F}{m^2}$$

$$= 1944\frac{A}{V^2} * 10^{-7}$$

$$= 194.4\frac{\mu A}{V^2}$$

(b) at Sat

$$I_D = \frac{1}{2}K_n'\frac{W}{L}V_{ov}^2$$

$$100 * 10^{-6} = \frac{1}{2} * 194.4 * 10^{-6} * \frac{8}{0.8}V_{ov}^2$$

$$V_{ov} = 0.32V = V_{GS} - V_T$$

$$\therefore V_{GS} = V_{ov} + V_t = 0.32 + 0.7 = 1.02V\ \#$$

In sat regim, since $V_{DS} \geq V_{GS} - V_T$

So $V_{DS\,min} = V_{GS} - V_T = V_{ov} = 0.32V$

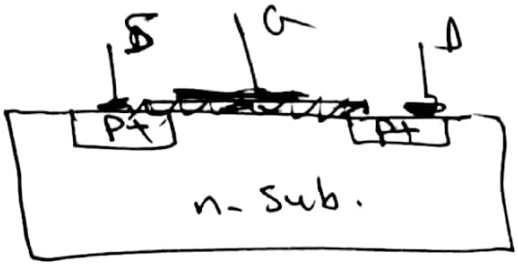
(c)

$$r_{DS} = \frac{1}{K_n'\frac{W}{L}V_{ov}}$$

$$1000 = \frac{1}{194.4 * 10^{-6}\frac{8}{0.8} * V_{ov}}$$

$$V_{ov} = 0.52 = V_{GS} - V_T$$

$$\therefore V_{GS} = V_{ov} + V_T = 0.52 + 0.7 = 1.22V$$

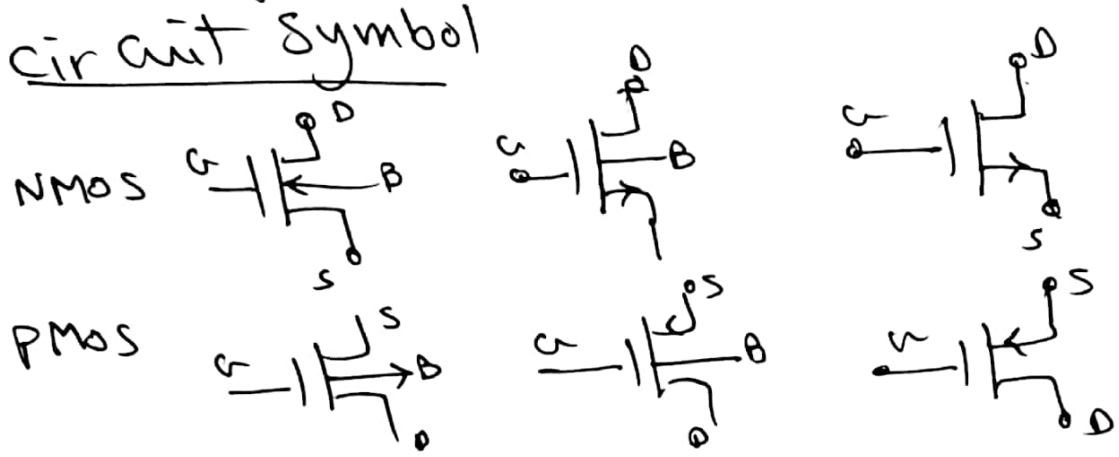


For PMOS

عكس الـ NMOS

PMOS is Complementary of NMOS

Circuit Symbol



For NMOS

① For Triode region

$V_{DS} < V_{GV}$ or $V_{DS} < V_{GS} - V_T$

أو $V_{GD} > V_T$

$$I_D = K_n' \frac{W}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$r_{DS} = \frac{1}{K_n' \frac{W}{L}(V_{GS}-V_T)} \equiv \frac{\partial V_{DS}}{\partial I_{DS}}$$ ↓ V_{DS} very small

② For Sat region

$V_{DS} \geq V_{OV}$, $V_{DS} \geq V_{GS} - V_T$

أو $V_{GD} \leq V_T$

$$I_D = \frac{1}{2} K_n' \frac{W}{L}(V_{GS}-V_T)^2$$

$V_{DS} < V_{GS} - V_T$
$V_{DS} - V_{GS} < -V_T$
$V_D - V_S - V_G + V_S < -V_T$
$-V_D + V_G > V_T$
$V_{GD} > V_T$

For PMOS

① Triode region

$V_{SD} < |V_{OV}|$, $V_{SD} < (V_{SG} - |V_{tp}|)$

أو $V_{DG} > |V_{tp}|$

$$I_D = K_p' \frac{W}{L}\left[(V_{SG}-|V_{tp}|)V_{SD} - \frac{V_{SD}^2}{2}\right]$$

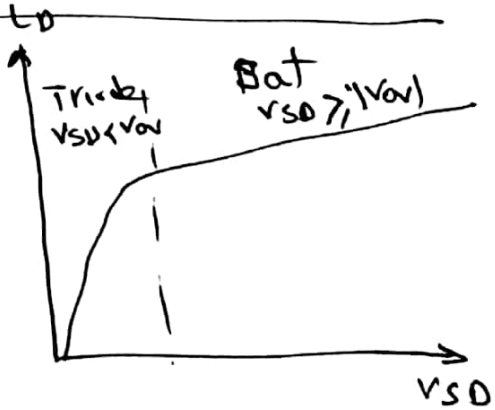
$$r_{DS} = \frac{1}{K_p' \frac{W}{L}|V_{OV}|}$$

② For Saturation region

$V_{SD} \geq |V_{OV}|$, $V_{SD} \geq |V_{SG} - |V_{tp}||$

أو $V_{DG} \leq |V_{tp}|$

$$I_D = \frac{1}{2} K_p' \frac{W}{L} V_{OV}^2 = \frac{1}{2} K_p' \frac{W}{L}(V_{SG}-|V_{tp}|)^2$$



10/10

L2S2

$$\frac{W}{L} = \frac{1}{k_n' r_{ds} (V_{GS} - V_T)} = \frac{1}{10^{-6} * 388.97 * 1 * 10^3 (1 - 0.5)}$$

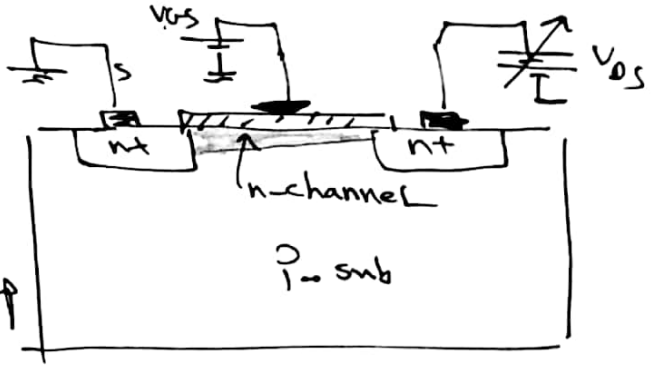
$$\frac{W}{L} = 5.1448$$

when $L_{min} = 0.18\,\mu m$

$$\therefore W = 5.91998 * 0.18 = 0.926\,\mu m$$

operation when v_{DS} increased

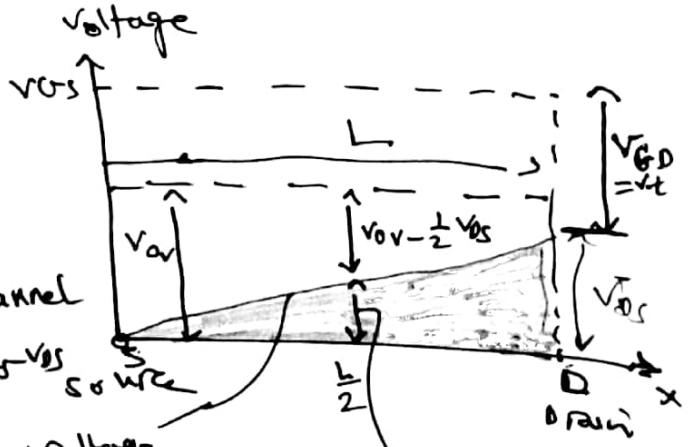
let v_{GS} held constant at value greater than V_t
or let MOSFET operate at constant overdrive value v_{ov}



Effect of Increase v_{DS}
make an effect on
channel shap

let v_{DS} appear as voltage drop
across the length of channel

as $v_{DS}\uparrow$ as channel be more Trapped



charge in the trapped channel
$\propto$ cross section area
voltage between gate & all points of channel
decrease from $v_{GS} = V_t + v_{ov}$ to $v_{GD} = v_{GS} - v_{DS}$

$$\therefore I_D \propto k_n' \frac{W}{L} v_{DS}$$

$$\text{area of channel} \propto \frac{[v_{ov} + (v_{ov} - v_{DS})]}{2}$$

$$\text{or} \propto \left(v_{ov} - \frac{v_{DS}}{2}\right)$$

$$\therefore I_D = k_n' \frac{W}{L} \left(v_{ov} - \frac{v_{DS}}{2}\right) v_{DS}$$